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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/643,895	08/18/2000	Quinn A. Jacobson	SUN-P4914	8680

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EXAMINER
O'BRIEN, BARRY J

ART UNIT	PAPER NUMBER
2183	5

DATE MAILED: 07/17/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/643,895	JACOBSON ET AL.
	Examiner	Art Unit
	Barry J. O'Brien	2183

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 August 0200 and 10 October 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☒ Claim(s) *2,5 and 6* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 August 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *2* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Claims 1-9 have been examined

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed on record in the file: Information Disclosure Statement as received on 10/10/2000.

Specification

3. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

4. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

5. The abstract of the disclosure is objected to because the word "comprising" is legal terminology that should not be included in an abstract. Correction is required. See MPEP § 608.01(b).

6. The abstract of the disclosure is objected to because it is unclear which register files the last line of the abstract references. Please change the sentence to finish reading "while not changing the size of the processor's register files themselves" to correctly comply with the references in the rest of the abstract. Correction is required. See MPEP § 608.01(b).

7. The disclosure is objected to because of the following informalities: Please replace the word "Baking" with "Backing" on line 12 of page 10. Appropriate correction is required.

Drawings

8. The drawings are objected to because of the following:

a. Figure 4 shows an "Instruction Stream" which is mentioned on page 13, lines 21 and 22, page 14, line 20 and page 15, line 6. Please include a reference number in both the specification and in the figure showing their correlation.

b. On line 18 of page 14, the reference number "410" of Figure 4 is cited. This reference number is not listed in Figure 4. Please correct with the appropriate reference number, or remove its reference from the specification.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

9. This application, filed under former 37 CFR 1.60, lacks formal drawings. Figures 1-5 include handwritten reference numbers. The informal drawings filed in this application are acceptable for examination purposes. When the application is allowed, applicant will be required to submit new formal drawings. In unusual circumstances, the formal drawings from the abandoned parent application may be transferred by the grant of a petition under 37 CFR 1.182.

Claim Objections

10. In claim 2 (line 15 of page 21), please change the phrase "each of said plurality of register files" to "each register file of said plurality of register files." This change ensures the correct claimed connectivity of lines 16-19 of page 21.

11. Claims 5b and 6b have unclear language. It is unclear in which order the decoding, the address availability, and the checking for both the number of addresses and the type of backing file instruction takes place. Please reword the paragraph to have a more direct voice by first adding the word "where" to the beginning of the "if said backing file instruction..." statement at the end of the paragraph and then moving it to directly after the "decoding said backing..." statement.

12. In claim 5, on line 3 of page 23, and in claim 6, on line 1 of page 24, the paragraph is labeled as "c" when it should be labeled as "d" in order to keep the correct numbered order. Please change this numbering error.

13. Claim 6d recites on line 4 of page 24, "if said backing register file instruction is of type load-backing-register-file." The claim describes a loading of main memory, so please replaced the above statement with "if said backing register file instruction is of type load-main-memory" as mentioned in claim 6b.

Claim Rejections - 35 USC § 112

14. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

15. Claims 7-9 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter

which applicant regards as the invention. The definition of a data structure is a physical or logical relationship among data elements, designed to support specific data manipulation functions (see MPEP Section 2106). In its broadest reasonable interpretation, a backing register file instruction by itself has no physical or logical relationships with other elements or data in a data structure as claimed. It is instead simply an instruction on a machine-readable medium (see also 35 USC 101 rejections below).

Claim Rejections - 35 USC § 101

16. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

17. Claims 7-9 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. "Machine readable medium" is non-statutory subject matter. The specification does not limit the definition of a machine to be a computer. If the applicant would like to change "machine readable medium" to "computer readable medium", the claims would then become statutory.

Claim Rejections - 35 USC § 102

18. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

19. Claims 1, 2, and 5 are rejected under 35 U.S.C. 102(b) as being anticipated by Sollars, U.S. Patent No. 5,900,025.

20. Referring to claim 1, Sollars teaches in Fig. 1 a processor 10 comprising at least one register file 22a,b, at least one execution unit 14, said at least one register file 22a,b operatively connected to said at least one execution unit 14 and a backing register file 20a operatively coupled to said at least one register file 22a, and where said backing register file 20a is operationally and responsively coupled to at least one user-visible instruction (see Col. 14, lines 37-52).

21. Referring to claim 2, Sollars teaches in Fig. 1 a processor as shown above 1 further comprising a plurality of register files 22a,b and further comprising at least one execution unit 14 operably connected to each register file 22a, 22b of said plurality of register files 22a,b and where said backing register file 20a is operably connected to each of said plurality of register files 22a,b providing thereby the ability to transfer values from any designated location in any designated register file 22a, 22b of said plurality of register files 22a,b to any designated location in said backing register file 20a, and from any designated location in said backing register file 20a to any designated location in any designated register file 22a, 22b of said plurality of register files 22a,b (See Col. 3, lines 32-34).

22. Referring to claim 5, Sollars teaches in Fig. 1a method for moving values from designated locations in designated register files 22a,b to designated locations in a backing register file 20a, and values in designated locations in said backing register file 20a to designated locations in designated register files 22a,b (see Col. 3, lines 25-34) comprising:

a. Identifying of a backing register file instruction in a sequence of instructions. While not stated explicitly, it is inherent in the decoding operation (Col. 6, lines 16-18) that the instruction be identified, for without the identification of an instruction a machine would only be able to execute at most one type of instruction, that which was hard-coded. It is also inherent that the "MOV" instruction performs the same functions as a backing register file (see Col. 14, lines 59-67), and the instruction contains both source and destination fields allowing the user to identify the specific register from and to which the transfer will take place (see Figs. 16b, 16c).

b. Decoding said backing register file instruction, making available addresses for specified numbers of locations in specified register files and an equal number of addresses for specified locations in said backing register file, where said number of addresses is at least one, if said backing file instruction is one of load-backing-register-file or load-register-file. Because the instructions describe the transfer of data from one register to another (see Col. 3, lines 25-34), it is inherent that not only must the instructions have at least one address for both the source and destination of the operation necessary for the instruction to execute encoded within it, but that there is a minimal amount of decoding that is necessary in order to extract these addresses.

c. Reading values from each of said addresses in said specified register file and writing said values to said equal number of addresses in said backing register file as specified by said backing register file instruction, if said backing register file instruction is of type load-backing-register-file. As mentioned above, the

instructions describe the transfer of data from one register to another (see Col. 3, lines 25-34). It is inherent that in the execute stage of an instruction's lifecycle that during a move/load-type instruction the data is moved from one specified address to another specified address using the addresses specified in the decoded instruction.

d. Reading values from each of said addresses specified in said backing register file and writing said values to said equal number of addresses in said specified register file, if said backing register file instruction is of type load-register-file. Again, as in part c, it is inherent that move/load-type instructions transfer data from one specified address to a second specified address extracted from the instruction.

23. Claim 6 is rejected under 35 U.S.C. 102(b) as being anticipated by Wilhelm et al, U.S. Patent No. 5,956,747.

24. Referring to claim 6, Wilhelm teaches a method for moving values from designated locations in main memory (32 in Fig. 2) to designated locations in a backing register file (28 in Fig. 2) and values in designated locations in said backing register file (28 in Fig. 2) to designated locations in main memory (32 in Fig. 2) comprising:

a. Identifying a backing register file instruction in a sequence of instructions. While not stated explicitly, it is inherent in the decoding operation performed by the Prefetch Unit (14 of Fig. 2 and Col. 4, lines 1-17) that the instruction be identified, for without the identification of an instruction a machine would only be able to execute at most one type of instruction, that which was hard-coded.

b. Decoding said backing register file instruction, making available addresses for specified numbers of locations in main memory and an equal number of addresses for specified locations in said backing register file, where said specified number of locations is at least one, if said backing register file instruction is one of load-main-memory or load-register-backing-file. Because more than one type of instruction will be required to transfer values between main memory and the backing register file, i.e. "load" and "store", it is therefore necessary that some sort of decoding operation take place to identify the type of instruction to be executed in order to execute a non-trivial program. One skilled in the art at the time of the invention would have recognized that an instruction to move values between a memory and a register file will be either of type "load" or "store" as described above, and will inherently contain the addresses necessary to correctly locate the source and destination locations encoded within the instruction.

c. Reading values from each of said addresses in said main memory and writing said values to said equal number of addresses in said backing register file as specified by said backing register file instruction, if said backing register file instruction is of type load-backing-register-file. For a "load" type instruction, the flow of data would be from the main memory to the backing register file. It is inherent in a "load" type instruction that upon execution, the value(s) are transferred from the source location to the destination location as specified by the decoded instructions data.

d. Reading values from each of said addresses specified in said backing register file and writing said values to said equal number of addresses in said main

memory as specified by said backing file instruction, if said backing register file instruction is of type load-backing-register-file. For a "store" type instruction, the flow of data would be from the backing register file to the main memory. It is inherent in a "store" type instruction that upon execution, the value(s) are transferred from the source location to the destination location as specified by the decoded instructions data.

Claim Rejections - 35 USC § 103

25. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

26. Claims 3 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sollars as applied to claims 1 and 2 above, and further in view of Wilhelm et al, U.S. Patent No. 5,956,747.

27. Referring to both claims 3 and 4, Sollars teaches a processor as in claims 1 and 2 (see above 35 USC 102 rejection), but does not include a connection circuit having a first and second connection, where said first connection is operably connected to said backing register file and said second connection is operably connected to a main memory. However, Wilhelm teaches a register file 28 and a register cache 52 operably connected to main memory 32 (see Fig. 2). The main memory is connected in such a hierarchy so that register values of the register files can be stored in any backing store memory (see Col. 5, lines 1-11). One skilled in the art at the time of the invention would know that in

order to execute a non-trivial program, one would need some sort of memory in order to store it within. One skilled in the art would also have realized that this memory would have to be abundant and cheap because of the size required to store a non-trivial program, thus discounting the idea of increasing the on-chip register file to the size needed as doing so would increase costs, slow performance, and increase the needed die area. It would therefore have been obvious to one skilled in the art at the time of the invention to operably connect a main memory to a backing register file.

Conclusion

28. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Barry J. O'Brien whose telephone number is (703) 305-5864. The examiner can normally be reached on Mon.-Fri. 8am-4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

BJO
July 14, 2003

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100